

ISSUE CLASSIFICATION	
Class	Subclass

PATENT NUMBER

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U.S. UTILITY Patent Application

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CLASS 423	SUBCLASS	ART UNIT	EXAMINER
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APPLICATION NO. 09/490705	CONT/PRIOR YES	CLASS 438 438	SUBCLASS 65	ART UNIT 1765	EXAMINER Moore
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ITS Kazuyoshi Ueno

Semiconductor device and a method for forming a via hole in a semiconductor device

CPA

PTO-2040
12/99

ISSUING CLASSIFICATION

[illegible]

<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) (Date)			NOTICE OF ALLOWANCE MAILED	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ _____ _____	_____ (Primary Examiner) (Date)				
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				Amount Due	Date Paid
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